PROF. AKKARY DEPT. OF ELECTRICAL AND COMPUTER ENGINEERING

AMERICAN UNIVERSITY OF BEIRUT

EECE 421 – COMPUTER Architecture

Quiz 2 – Fall 2012

NAME:

_____

ID: _____

INSTRUCTIONS:

- **THE DURATION OF THE EXAM IS 120 MINUTES. NO TIME EXTENSION.**
- **THE EXAM IS CLOSED-BOOK/CLOSED-NOTES.**
- **USING CELL PHONES IS NOT ALLOWED IN THE EXAMINATION ROOM.**
- **WRITE YOUR NAME AND ID. NUMBER IN THE SPACE PROVIDED ABOVE.**
- **CIRCLE ONLY ONE ANSWER.**
- **READ THE QUESTIONS CAREFULLY BEFORE ANSWERING.**
- **IN SOME QUESTIONS, MORE THAN ONE CHOICE MAY BE A VALID ANSWER. CIRCLE THE BEST CHOICE YOU THINK IS THE MOST APPROPRIATE ANSWER TO THE QUESTION.**
- **ALL QUESTIONS ARE EQUALLY WEIGHTED.**
- **THERE IS NO PENALTY FOR WRONG ANSWERS.**
- **USE THE BACK PAGES FOR SCRATCH IF NEEDED**
- **CHECK THAT YOU HAVE A TOTAL OF 3 PAGES.**
- **NO QUESTIONS ARE ALLOWED.**
- **YOU CANNOT LEAVE THE EXAM ROOM FOR ANY REASON UNTIL YOU COMPLETE THE EXAM.**

(1) Which of the following statements is **FALSE**:

In extended Tomasulo's algorithm, which uses a reorder buffer,

a. The reorder buffer is used to provide precise state in case of an interrupt or mispredicted branch.
b. The ID of the reservation station in which an instruction is written is used as a tag.
c. The tag is written into the register destination entry in the Register File and a busy bit is set in the entry when the instruction is decoded and then written into the reservation station.
d. The decoded instruction is allocated an entry in the reorder buffer in program order.
e. Results are written into the reorder buffer after execution.

(2) Which of the following statements is **FALSE**:

In extended Tomasulo's algorithm, which uses a reorder buffer,

a. After an instruction is decoded, its assigned tag is written into the register destination entry in the Register File and a busy bit is set in the entry.
b. An instruction reads its source operand data from the register file entry if the entry is not busy.
c. If the source operand register entry is busy, the tag in the register entry is read and carried with the instruction into the reservation station.
d. The reservation station uses data tags to identify and grab the data from the common data bus.
e. Results are written into the reorder buffer after execution.

(3) Which of the following statements is **FALSE**:

In extended Tomasulo's algorithm, which uses a reorder buffer,

a. The busy bit in a register entry is set to "BUSY" every time a tag is written in the entry.
b. The busy bit in a register entry is cleared to change the state to "NOT BUSY" every time data is written into the register entry.
c. Data is written to the reorder buffer out-of-order.
d. Data is moved from the reorder buffer into the register file in program order.
e. Instructions read source operand data or tags from the register file in program order.

(4) Which of the following statements is **TRUE**:

a. The reorder buffer was first used in Tomasulo's algorithm.
b. Most microprocessors that feature out-of-order execution use a future file.
c. Instructions read operands from the reorder buffer in-order.
d. A history buffer provides better performance than a future file.
e. Instructions write results to the reorder buffer in-order.

(5) Which of the following statements is **FALSE**:

a. Pentium Pro used reorder buffer for register renaming.
b. Pentium Pro converted all CISC instructions to RISC using one complex decoder and 2 simple decoders.
c. Pentium Pro was 3-wide superscalar.
d. Pentium Pro used one centralized set of reservation stations.
e. Pentium Pro used a BTB for branch prediction.

(6) A branch predictor uses saturating counters state machines. The branch predictor state corresponding to a branch being predicted is 01 and the branch is mispredicted. The next state will be:

a. 00
b. 01
c. 10
d. 11
e. Need more information to determine the next state.

(7) Which of the following statements is **TRUE**:

a. The reorder buffer has entries for every instruction including instructions that do not write any registers, such as branches and stores.
b. Most microprocessors that feature out-of-order execution use a future file.
c. A history buffer provides better performance than a reorder buffer.
d. Instructions read operands or tags from the reorder buffer in program order.
e. Instructions write results to the reorder buffer in-order.

(8) Choose the pair of terms that are most related:

a. History buffer, branch predictor
b. History buffer, branch target buffer
c. History buffer, branch mispredictions
d. History buffer, register renaming
e. History buffer, Pentium Pro processor

(9) Which of the following statements is **TRUE**:

a. The Pentium Pro processor implements a long pipeline with 2 distinct sections.
b. The Pentium Pro processor implements a long pipeline with 3 distinct sections.
c. The Pentium Pro processor implements a long pipeline with 4 distinct sections.
d. The Pentium Pro processor implements a 4 wide superscalar pipeline.
e. None of the above is TRUE.

(10) Which of the following statements is **FALSE**:

a. A branch target buffer is typically used to predict the target address of conditional branches.
b. A branch target buffer is typically used to predict the target address for all branches.
c. A branch target buffer is used to store branch target addresses.
d. A branch target buffer is sometimes used to predict the outcome of branches.
e. A branch target buffer is indexed by the PC of a branch.

(11) A correlating branch predictor uses 7 history bits and 8 address bits. The size of the state machines array is:

a. 128 entries
b. 256 entries
c. 384 entries
d. 32K entries
e. None of the above.